



# W/C  
843.37558VX1  
Response Under 37 CFR 1.116  
Expedited Procedure  
Group No.: 2825  
2-403

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

**Applicant:** M. FUNABASHI

**Application No.:** 09/902,673

**Filed:** July 12, 2001

**For:** **METHOD OF MANUFACTURING A SEMICONDUCTOR  
INTEGRATED CIRCUIT DEVICE**

**Art Group:** 2825

**Examiner:** L. Malsawma

RECEIVED  
FEB - 3 2003  
TC 2800 MAIL ROOM

**AMENDMENT AFTER FINAL REJECTION**

**ATTN: BOX AF**  
Commissioner for Patents  
Washington, D.C. 20231

January 29, 2003

Sir:

In response to the Office Action mailed July 29, 2002, the time period for responding having been extended until January 29, 2003, please amend the above-identified application as follows:

**IN THE CLAIMS:**

Please cancel claim 31 without prejudice or disclaimer, and add the following new claim to the application.

--33. A method of manufacturing a semiconductor integrated circuit device according to claim 20, wherein said processing solution etches the silicon oxide but does not etch the silicon wafer.--

Do not enter